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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/522,470	03/09/2000	Hiroshi Katakura	000267	3147

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	11

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No. 09/522,470	Applicant(s) KATAKURA ET AL.	
	Examiner Chat C. Do	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7,8,13 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 8,13-14* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This communication is responsive to Amendment B, filed 7/24/2003.

2. Claims 1-2, 7-8, and 13-14 are pending in this application. Claims 1-2, 7, and 13-14 are independent claims. In Amendment, claims 13-14 are added. This action is made final.

Claim Objections

3. Claim 14 is objected to because of the following informalities:

Claim 14 is written exact the same as claim 2. The applicant is advised to either distinguish from claim 2 or delete claim 14.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 7 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 7, the added limitation "first outputting section...the first resulting signal" is mis-descriptive because the first NAND actually outputs the first resulting signal and the second NAND actually outputs the second resulting signal. For the examination purposes, the examiner considers this limitation as cited above.

Re claim 13, the limitation "the controllable selection signal" lacks an antecedence basis. For examination purposes, the examiner considers this limitation as "a controllable selection signal".

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2, 8, and 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Freeman (Re. 34,363).

Re claim 1, Freeman discloses in Figure 2 a logic circuit comprising: a first inversion section (21) for inverting a first input signal (A) having one of positive logic and negative logic and outputting the inverted signal (bar(A)); a second inversion section (22) for inverting a second input signal (B) having the other the positive logic and the negative logic and outputting the inverted signal (bar(B)); and a transmission section (transmission lines that connect all signals to 23-26) for selectively outputting one of the inverted first input signal of first inversion section (output controls by C2 and bar(C2)) and the inverted second input signal of second inversion section (output controls by C3 and bar(C3)) in accordance with a logical value which depends upon an externally controllable selection signal (Cs) and an inverted signal of the selection signal (bar(Cs)).

Re claim 2, it has the same limitation cited in claim 1. Thus, claim 2 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 8, Freeman further discloses in Figure 2 comprising a first switching section (area including transmission lines of A, bar(A) and C2, bar(C2)) provided on an input side of first inversion section (21) and capable of performing switching of whether the first input signal should be passed (on) or blocked (off) in accordance with an external control signal (bar(C2)); and a second switching section (area including transmission lines of B, bar(B) and C3, bar(C3)) provided on an input side of second inversion section (22) and capable of performing switching of whether the second input signal should be passed (on) or blocked (off) in accordance with the external control signal (bar(C3)).

Re claim 13, Freeman further discloses in Figure 2 a first inversion section (21) for inverting a first input signal (21) having one of positive logic and negative logic and outputting an inverted first input signal (bar(A)), first inversion section (21) being essentially composed of transistor circuits (col. 4 lines 45-55) each of transistor circuits having a first input signal terminal (input of 21) for the first input signal (A), a first input selection signal terminal (e.g 29c) for the controllable selection signal (e.g C1) and an outputting terminal (input to 23) for outputting the selection signal (C2) or the inverted signal (bar(C2)) based on the logic of the first input signal (A); a second inversion section (22) for inverting a second input signal (B), second inversion section (22) being essentially composed of transistor circuits each (col. 4 lines 45-55) of transistor circuits having a second input signal terminal (input to 22) for the second input signal (B), a

second input selection signal terminal (e.g. 29d) for the controllable selection signal (e.g. C0) and an outputting terminal (input to 25) for outputting the selection signal (C3) or the inverted signal (bar(C3)) based on the logic of the first input signal; and a transmission section (all the connection bus between inverters to other logic components) for selectively outputting one of the output of first inversion section (21) and the output of second inversion section (22) in accordance with a logical value which depends upon an externally controllable selection signal (C2 and C3) and an inverted signal of the selection signal (bar(C2) and bar(C3)).

Re claim 14, it has the same limitations cited in claim 2. Thus, claim 14 is also rejected under the same rationale in the rejection of rejected claim 2.

Allowable Subject Matter

8. Claim 7 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Response to Arguments

9. Applicant's arguments with respect to claims 1-2, 7-8, and 13-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Chat C. Do
Examiner
Art Unit 2124

August 28, 2003

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100